

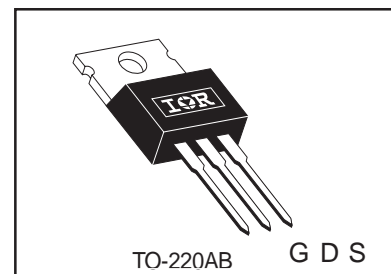
**Applications**

- Switch Mode Power Supply ( SMPS )
- Uninterruptable Power Supply
- High speed power switching

<b>V<sub>DSS</sub></b>	<b>R<sub>ds(on)</sub> max</b>	<b>I<sub>D</sub></b>
<b>500V</b>	<b>1.40Ω</b>	<b>5.0A</b>

**Benefits**

- Low Gate Charge Q<sub>g</sub> results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss specified ( See AN 1001)



**Absolute Maximum Ratings**

	<b>Parameter</b>	<b>Max.</b>	<b>Units</b>
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	5.0	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	3.2	
I <sub>DM</sub>	Pulsed Drain Current ①	20	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	74	W
	Linear Derating Factor	0.59	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	5.3	V/ns
T <sub>J</sub>	Operating Junction and Storage Temperature Range	-55 to + 150	°C
T <sub>STG</sub>	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

**Typical SMPS Topologies:**

- Two transistor Forward
- Half Bridge and Full Bridge

Notes ① through ⑤ are on page 8

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# IRF830A

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.60	—		$V/^\circ\text{C}$ Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.4	$\Omega$	$V_{GS} = 10V, I_D = 3.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25 250	$\mu A$	$V_{DS} = 500V, V_{GS} = 0V$ $V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	2.8	—	—	S	$V_{DS} = 50V, I_D = 3.0A$
$Q_g$	Total Gate Charge	—	—	24	nC	$I_D = 5.0A$ $V_{DS} = 400V$ $V_{GS} = 10V$ , See Fig. 6 and 13 ④
$Q_{gs}$	Gate-to-Source Charge	—	—	6.3		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	11		
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 250V$ $I_D = 5.0A$ $R_G = 14\Omega$ $R_D = 49\Omega$ , See Fig. 10 ④
$t_r$	Rise Time	—	21	—		
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		
$t_f$	Fall Time	—	15	—		
$C_{iss}$	Input Capacitance	—	620	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ , See Fig. 5 $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 400V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 0V$ to $400V$ ⑤
$C_{oss}$	Output Capacitance	—	93	—		
$C_{riss}$	Reverse Transfer Capacitance	—	4.3	—		
$C_{oss}$	Output Capacitance	—	886	—		
$C_{oss}$	Output Capacitance	—	27	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	39	—		

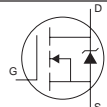
## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	230	mJ
$I_{AR}$	Avalanche Current①	—	5.0	A
$E_{AR}$	Repetitive Avalanche Energy①	—	7.4	mJ

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.7	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	5.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	20		
$V_{SD}$	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 5.0A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	430	650	ns	$T_J = 25^\circ\text{C}, I_F = 5.0A$
$Q_{rr}$	Reverse Recovery Charge	—	2.0	3.0	$\mu\text{C}$	$di/dt = 100A/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

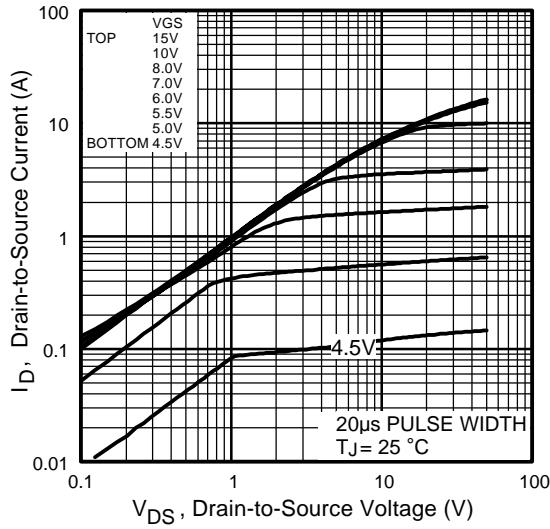


Fig 1. Typical Output Characteristics

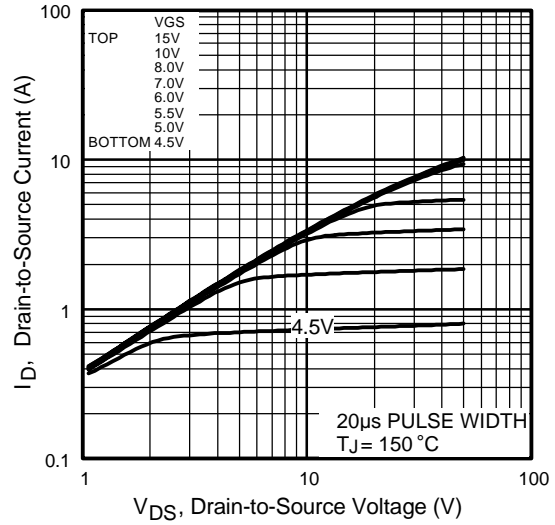


Fig 2. Typical Output Characteristics

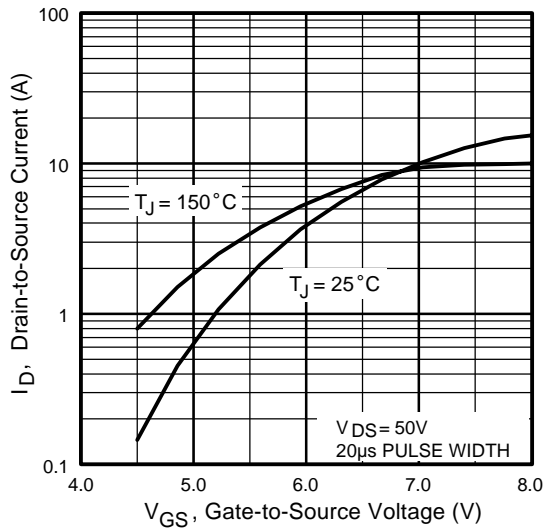


Fig 3. Typical Transfer Characteristics

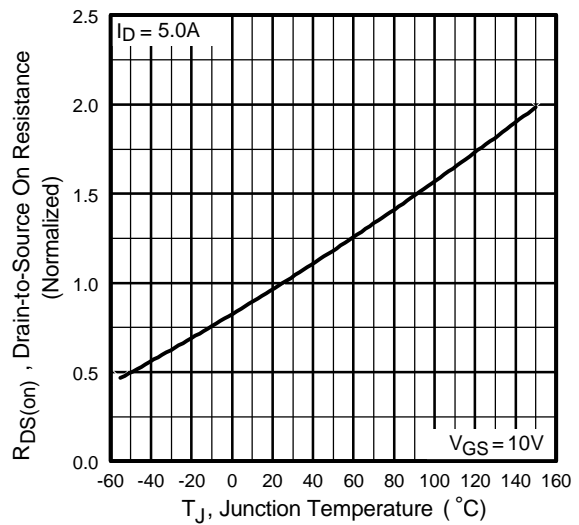
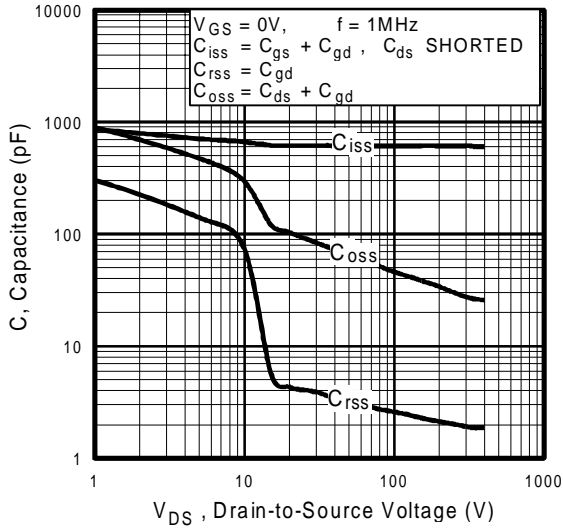
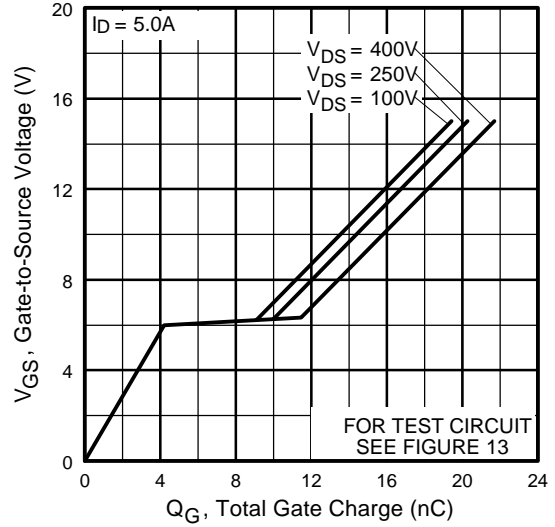


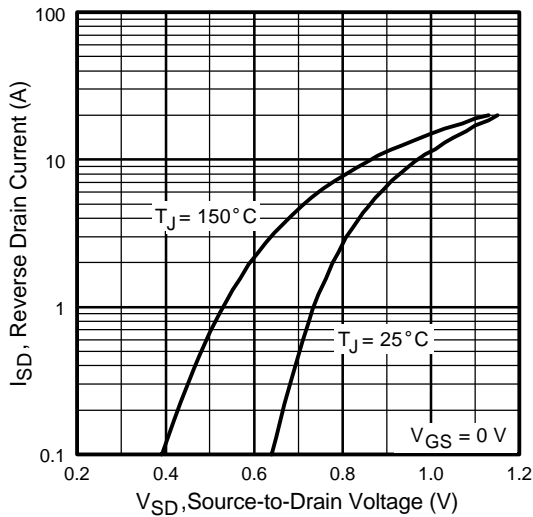
Fig 4. Normalized On-Resistance Vs. Temperature



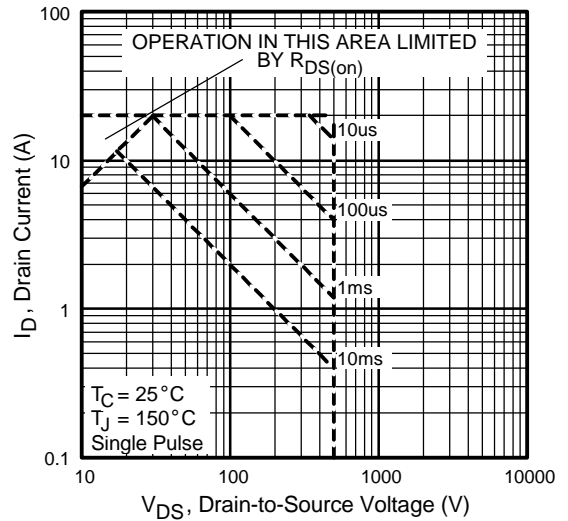
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



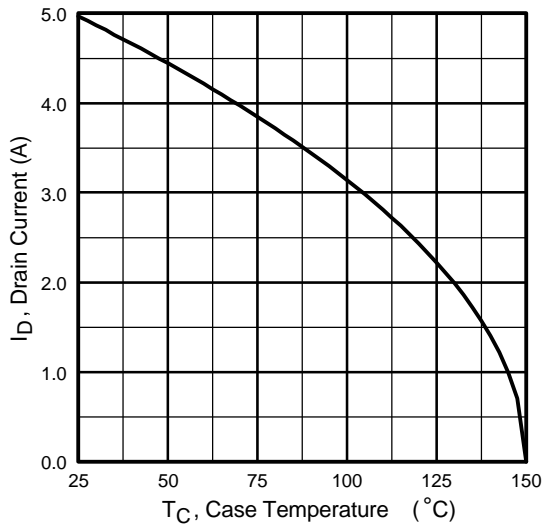
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



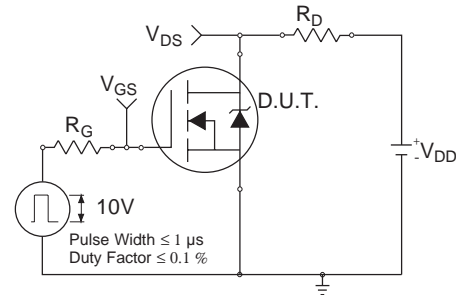
**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area



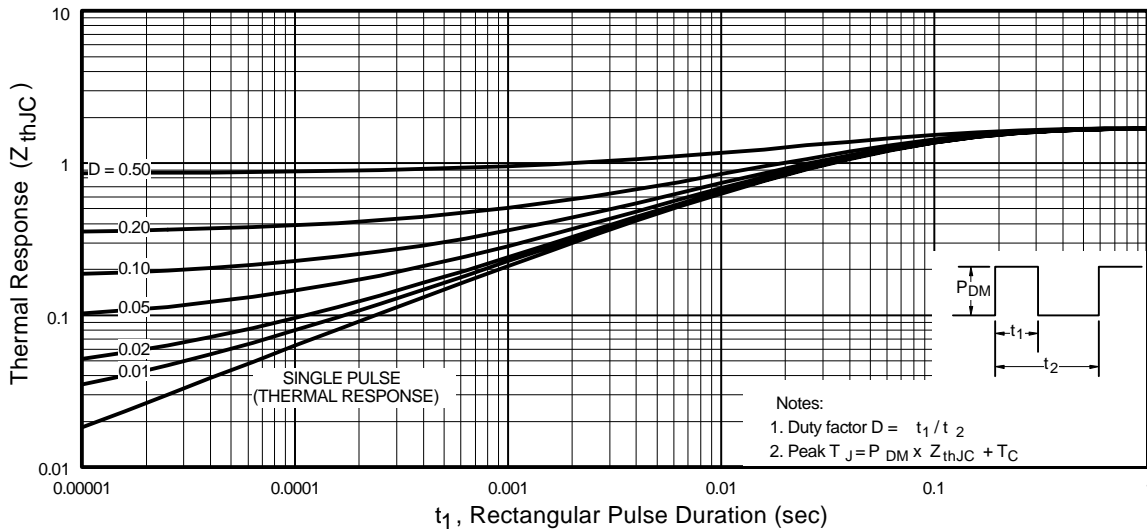
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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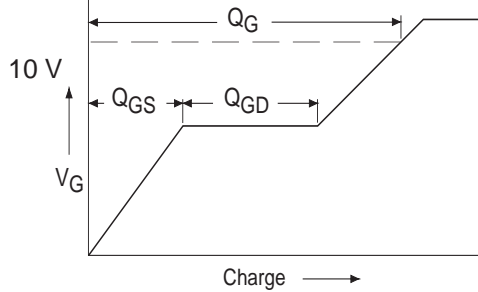
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**Fig 12a.** Unclamped Inductive Test Circuit



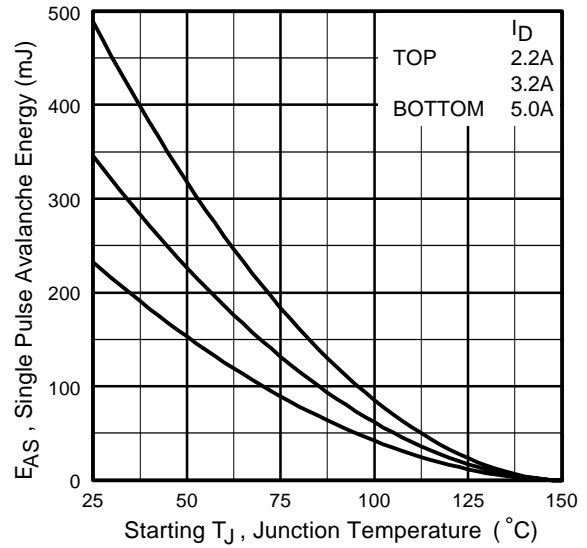
**Fig 12b.** Unclamped Inductive Waveforms



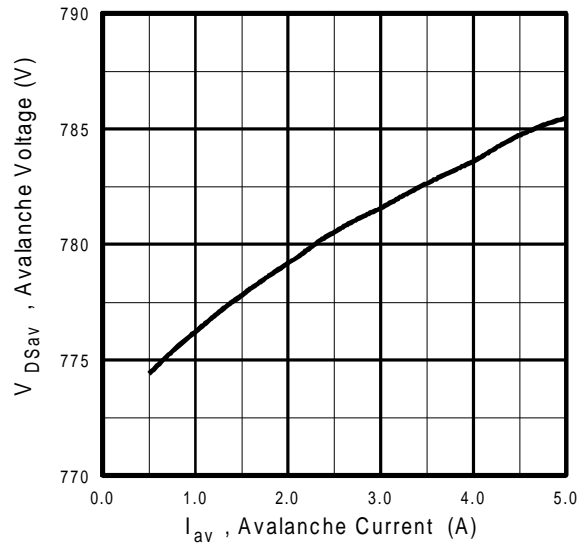
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 12d.** Typical Drain-to-Source Voltage Vs. Avalanche Current

**Peak Diode Recovery dv/dt Test Circuit**



\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

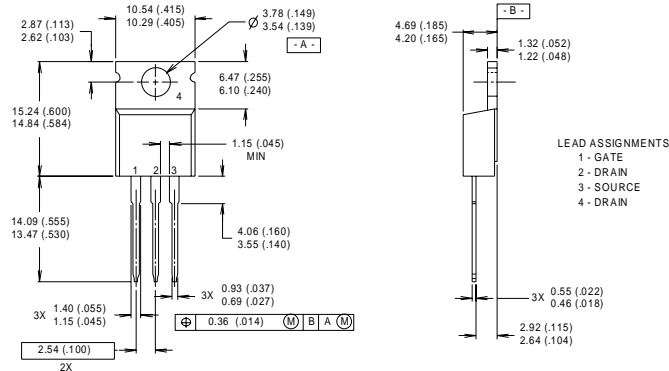
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## Package Outline

### TO-220AB Outline

Dimensions are shown in millimeters (inches)

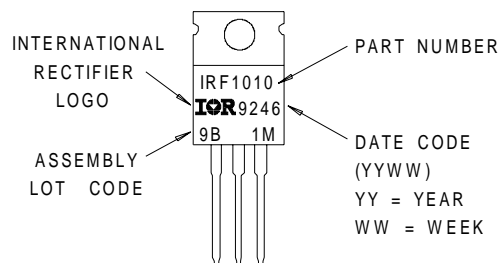


- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
  - 2 CONTROLLING DIMENSION : INCH
  - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
  - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## Part Marking Information

### TO-220AB

EXAMPLE : THIS IS AN IRF1010  
WITH ASSEMBLY  
LOT CODE 9B1M



### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 18\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 5.0\text{A}$ . (See Figure 12)
- ③  $I_{SD} \leq 5.0\text{A}$ ,  $di/dt \leq 370\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$

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**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
**IR EUROPEAN REGIONAL CENTRE:** 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000  
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